

PROGRAMMABLE LOGIC APPLICATION NOTES

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This column will be provided each quarter as a source for reliability, radiation results, NASA capabilities, and other information on programmable logic devices and related applications. This quarter will start a series of notes concentrating on analysis techniques with this issues section discussing worst-case analysis requirements. If you have information that you would like to submit or an area you would like discussed or researched, please give me a call or e-mail.

2000 MAPLD Conference
September 26-28, 1999
Kossiakoff Conference Center
JHU/Applied Physics Laboratory
Laurel, Maryland

The 3rd annual Military and Aerospace Applications of Programmable Devices and Technologies Conference will address devices, technologies, usage, reliability, fault tolerance, radiation susceptibility, and applications of programmable devices and adaptive computing systems in military and aerospace systems. The program will consist of approximately 60 oral and poster technical presentations and 20 industrial exhibits. The majority of the conference is open to US and foreign participation and is unclassified. There will be one classified session at the secret level, for U.S. citizens only. For conference information, please see Programmable Technologies Web Site (<http://rk.gsfc.nasa.gov>).

At the time of this printing, the oral presentations will have been selected. Submissions for poster papers and industrial exhibits will still be accepted and authors may submit abstracts.

The invited speaker program features an excellent set of talks. This includes Eldon Hall, a designer of the Apollo Guidance Computer (AGC), the keynote address by space historian Henry Spencer, and Tom Jones, NASA astronaut. Dr. Massengill of Vanderbilt University will discuss emerging technologies and J. Kinnison of JHU/APL will be our AIAA invited speaker. More information and abstracts are available at:

<http://rk.gsfc.nasa.gov/richcontent/MAPLDCon00/InvitedSpeakers00.html>

Presenters this year will have the option of having their work, subject to peer review, published in the AIAA **Journal of Spacecraft and Rockets**. The special editor is Dr. Tanya Vladimirova of the University of Surrey.

We also wish to acknowledge our new conference sponsor, the IEEE Aerospace & Electronic Systems Society.

Registration for the conference is now open. Please see:

<http://rk.gsfc.nasa.gov/richcontent/MAPLDCon00/Reg/Registration.html>

What's New?

A large amount of data, reports, papers, application notes, and conference information are being stored on our companion Programmables Technology www site, <http://rk.gsfc.nasa.gov>. In order to make it easier to keep readers up to date, all new additions to the site are being listed, in chronological order on our "What's New" page. This can be found at:

http://rk.gsfc.nasa.gov/What's_New.htm

Analysis Techniques

The following application note on worst-case analysis requirements was contributed by Dr. R. L. Barto of Spacecraft Digital Electronics. In 1991 Dr. Barto received the NASA Public Service Medal for the Galileo AACCS design. This note is the first in a series on analysis techniques.

An Outline of Worst-Case Analysis Requirements for Digital Electronics

Every designer's goal is mission success: the production of a correctly functioning system. One of the keys to achieving that goal is the worst case analysis (WCA). A detailed WCA, if performed during the design phase, can find design problems that may not be found during the test phase. Timing errors, interface margin problems, and other design flaws may manifest themselves only under limited operating conditions that are not present during test, such as temperature extremes, age, or radiation, or in limited operating modes that are not exercised in test. The only way to guarantee that no design flaws exist

in a circuit is to carefully analyze the circuit and prove their absence.

The purpose of a WCA is to prove the design will function as expected during its mission. The spirit of analysis is proof: all circuits are considered guilty of design flaws until proven innocent. The following is an outline of WCA requirements, which introduces the circuit design items that must be reviewed as part of the WCA.

1. Part Parameters and Deratings

Data book part parameters often do not match the part's intended operating environment. Each parameter must be derated from the data book value for the intended environment to compensate for the effects of temperature, age, voltage, and radiation where applicable. A derating for excess load capacitance must also be given when high capacitive loads are driven. This information forms the database on which the analysis is performed.

2. Timing analysis

A complete timing analysis will contain, for each clocked device in the system, a proof that all of the derated timing parameters are met:

- 2.1 Set-up and hold times at all clocked inputs, including the data inputs, synchronous sets, clears, and enables, and any inputs for which a set-up or hold time is specified;
- 2.2 Pulse widths of clocks, and asynchronous set, clear, and load inputs, and any input for which a pulse width is specified;
- 2.3 Set and clear recovery time -- the set-up time from the release of an asynchronous set or clear until the next clock edge.

In addition, all clock inputs and a synchronous inputs such as sets, clears, and loads must be shown to be free from both static (010 or 101) and dynamic (001011 or 110100) hazards.

- 2.4 CMOS Parallel Clocking
- 2.5 Timing of Analog Circuitry
- 2.6 Minimum Propagation Delays
- 2.7 Calculation of Pulse Shortening
- 2.8 Consideration of Transition Times in Delay Calculations

3. Gate Output Loading

The analysis must show that no gate output drive capacities have been exceeded. Unusually high

output drive currents may affect output voltage levels and propagation delays, and may cause thermal problems resulting in part damage.

4. Interface Margins

The interface margin analysis must show that all of the gates have their input logic level thresholds met. For gates within the same family, and assuming no unusual loading, this analysis is only a formality. However, where different families, or digital and analog parts, interface, each different class of interfaces must be analyzed. Decreased interface margins cause circuits to be more susceptible to noise and can affect the operation of some parts.

- 4.1 CMOS to Non-CMOS Interfaces
- 4.2 Variation of CMOS I_{CC} With Input Voltage Level
- 4.3 Input Transition Times
- 4.4 Input Requirements of Analog Devices
- 4.5 Driving Mixtures of TTL and CMOS

5. State Machine Transitions

State machines must be analyzed to assure that they will not exhibit anomalous behavior, such as system lock-up.

- 5.1 Unused States
- 5.2 Simultaneous Assertion of Flip-Flop Sets and Clears
- 5.3 Asynchronous State Machines
- 5.4 Reset Conditions and Homing Sequences

6. Asynchronous Interfaces

An asynchronous interface is one for which the set-up and hold times of incoming signals at receiving latches or flip-flops cannot be guaranteed. An example is data generated on one clock being transferred to flip-flops on a second clock having no synchronous relationship to the first, even if the two clocks have the same frequency. The analysis must show either that asynchronous signals are properly synchronized to the appropriate clock or that the circuitry receiving asynchronous signals will function correctly if set-up and hold times are not met.

7. Reset Conditions and Generation

All circuitry must be shown to be placed into a known state during reset. The width of the reset pulse should be longer than the longest reset T_{PW} specified for any of the parts. In general, a reset should be treated as an asynchronous input to a

sequential circuit and should be synchronized with the clock used by the devices being reset.

- 7.1 Reset Duration vs. Supply Voltage Level and Ramp-up Timing
- 7.2 Unintended Execution of External Commands on Power-up and After Reset
- 7.3 Synchronous Resets and Oscillator Start-up Time
- 7.4 Reset Release Timing

8. Part Safety Conditions

The analysis must prove that the circuit is designed to prevent its parts from being damaged. Part damage can result from a design which does not protect ESD sensitive parts, allows interfaces between incompatible parts families, or fails to provide for other requirements of the parts.

- 8.1 Protection of ESD Sensitive Parts
- 8.2 Input Voltage Levels
- 8.3 Tri-State Output Overlap
- 8.4 Floating Inputs
- 8.5 Use of Internal IC Protection Diodes
- 8.6 Use of Parts Outside of Manufacturers' Recommendations

9. Cross-Strap Signals Between Redundant Modules

The requirements for cross-strap signals can be derived from their basic purpose, that of fault isolation. It must therefore be shown that isolation between boxes is actually achieved.

- 9.1 Undesirable Powering of Modules via Cross-Strap Circuitry
- 9.2 Sharing of Cross-Strap Gates

10. Circuit Interconnections

The analysis must show that circuit interconnection requirements are met from the standpoint of signal quality as affected by edge rates, loading, and noise. Circuits of interest here include connections on and between PC boards and with peripheral units.

- 10.1 Termination of High Edge-Rate Signals
- 10.2 Off- Board Connections of Edge-Sensitive Inputs
- 10.3 Edge Rates of Harness Signals
- 10.4 Calculation of Harness Noise Threat Model
- 10.5 Noise Susceptibility Analysis of Input Circuitry
- 10.6 Drivers and Receivers for Off-board Signals

11. Bypass Capacitance Analysis

The analysis must show that the amount of on-board bulk and bypass capacitance is appropriate for the circuitry. The analysis will consider power supply line inductance, circuit operating frequency, and component current requirements. The choice of capacitors must be shown appropriate based on their frequency response.

Conclusion

A complete WCA contains an analysis of many circuit requirements that will be difficult or impossible to prove met by test. The correct time to perform the analysis is during the design phase. Putting off the analysis until after the design is completed invites costly redesign and system failure that could be avoided by doing the analysis before the hardware is built.

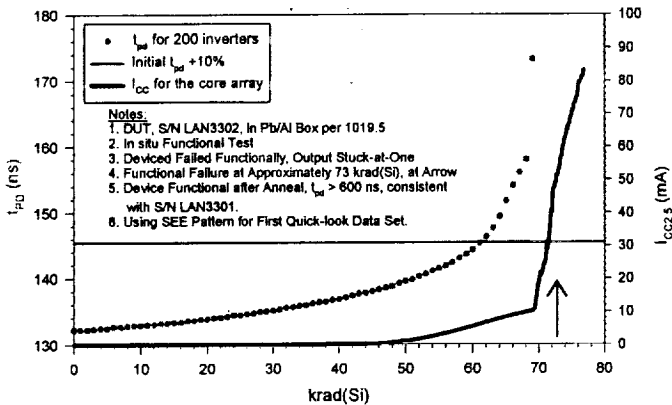
Nonvolatile, Reprogrammable FPGA Data

Two Actel A500K050 prototype FPGAs were subjected to a total dose test. These devices, packaged in PQFP208 packages, were irradiated at 1 krad(Si)/Hour at the NASA/GSFC total dose facility. The test pattern for this first look was primarily designed for an SEE evaluation. A serial string of inverters was included in the design to enable delta t_{PD} measurements for an initial assessment of total dose performance. An initial SEE evaluation should be completed by press time for this column.

The A500K050 is the smallest device in this series, with 43,000 "typical gates." The data sheet shows the A500K510 as the largest with 410,000 "typical gates." These devices are reprogrammable and nonvolatile. Flash technology is utilized for the switch and no boot device is required. The data sheet claims the device is "live at power-up." The device implements the TRST* pin as part of the IEEE 1149.1 JTAG TAP controller. The logic array of this device utilizes a 2.5 VDC power supply. A bias voltage of 3.3 VDC was also supplied.

The first device, S/N LAN3301, was used to obtain an initial understanding of the characteristics of this new technology. Several results came from this first run. First, I_{CC} , by itself, was not a good predictor of performance. Secondly, there was a significant degradation in t_{PD} as a function of total dose. After

the first run, it was found that t_{PD} increased by several times. Consequently, the instrumentation plan for S/N LAN3302 was developed. For this test, *in situ* measurements were made of I_{CC} , functionality (using the inverter string), and t_{PD} . I_{CC} was monitored at 5 minute intervals with an over current protection circuit constantly enabled. Functionality and t_{PD} was measured at 1 krad(Si) intervals. After completion of the test, a full functional test was made in the lab.



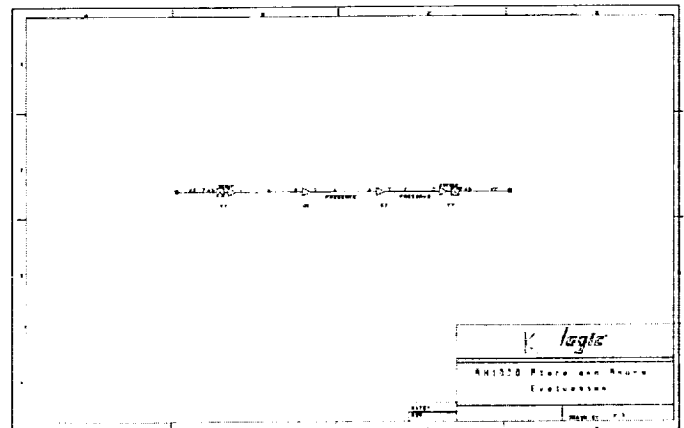
The data from the S/N LAN3302 run is shown in the figure above. At the completion of the run, functional failure was found, at a modest current level. The chart includes a reference line at a level corresponding to a +10% increase in t_{PD} from the initial value. This is frequently the limit used by analysts for delta propagation delay so makes a convenient reference point. It is seen that this limit is exceeded at the moderately low level of I_{CC} of approximately 6 mA.

P&R and Propagation Delay

Previous application notes have discussed the use of local, high-skew clocks for elements such as shift registers and parallel counters. In general, one should use the global, low-skew clocks that the manufacturer provides. In some cases, however, that is either not possible or not desirable. For example, a low power circuit may not wish to drive the entire global clock network for only a few flip-flops. In other cases, the system design may require more clocks than are present in the device being used. There are reliable techniques for designing with high-skew clocks such as opposite edge clocking for edge-triggered flip-flops and use of a two-phase non-overlapping clock for latches. Unfortunately, many designs still utilize a single edge, single-phase clock and a high-skew route.

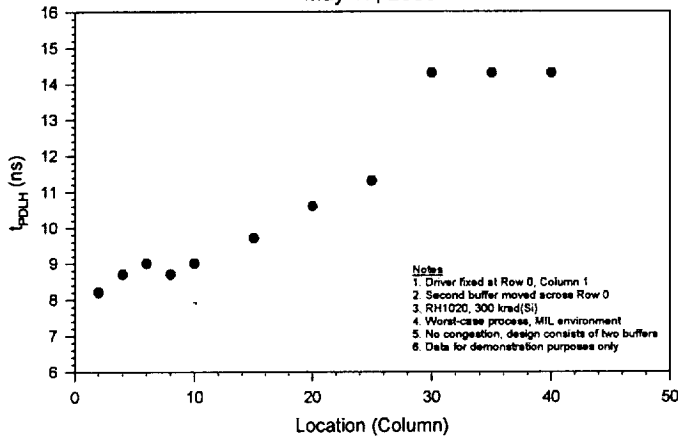
The term "sequentially adjacent" refers to two flip-flops clocked by the same clock that are connected by combinational logic and routing. If they are triggered on the same edge, then it is required, for reliable operation, that the minimum propagation delay ($t_{CLK \rightarrow Q} + t_{ROUTE}$) be greater than the maximum clock skew and t_H . Although a "wire" on a schematic drawing appears as a wire, when implemented in an FPGA there can be considerable delay transporting a signal across a wire. This delay is dependent on the placement and routing and the particular microcircuit. Note that for Actel FPGAs, for example, the resistance of an antifuse will vary from microcircuit to microcircuit and must be treated as a random variable.

As a demonstration for the effects of placement and routing, a simple design consisting of two buffers was analyzed. The RH1020 was used and the conditions were set to worst-case, 300 krad(Si), and MIL standard voltage and temperature. The RH1020 consists of 14 rows and 44 columns. The time measured, t_{PDLH} , was from the input of the first buffer to the input of the second one. The preserve property was used so that the Combiner would not eliminate any of the logic elements. The first buffer, G1, was fixed at Row 0, Column 1. The second buffer, G2, was varied in position. For each change in position, the place and route tools were run with standard settings. The times reported are in a sense "best-case" since the virtually empty chip will ensure that there was no routing congestion and all routing segments were available. The numbers shown here are for demonstration purposes only. For an actual design, post-layout extracted parameters should be used.



The first run moved buffer G2 down Row 0. The effects on propagation delay are shown in the chart below. While the data is clearly not monotonic, it is seen that in general the delays increase as the buffers are separated, as would be expected. Additionally, once a certain distance is exceeded, there is no further increase in propagation delay. By moving the location of the buffer G2, the propagation delay can increase by almost a factor of 2.

RH1020 P&R Analysis
Effect of Row Position on Prop Delay
May 17, 2000

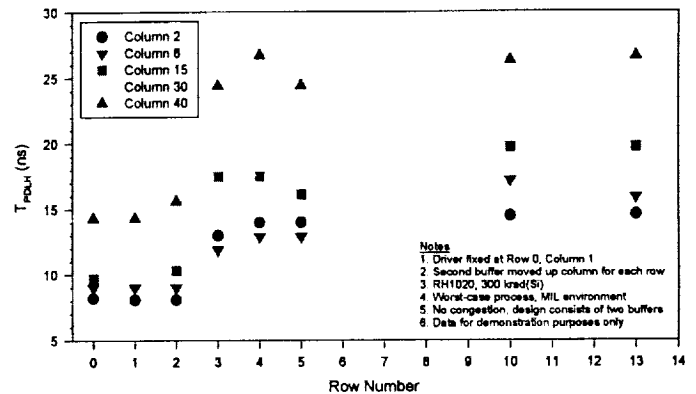


Next, the effects of placing a buffer in different rows was examined. That is, for a fixed column difference, how does the row selection effect propagation delay? Again, the buffer G1 was fixed at Row 0, Column 1. Individual sets of runs were made with the buffer G2 moving up Columns 2, 6, 15, 30, and 40. The results are shown in the chart below. The data for columns 30 and 40 were identical.

Again, we see that the data in general increases, although not monotonically for the points analyzed. The data also shows the sensitivity in moving the receiving buffer in the Y direction - increasing Row number. After two rows, there is a step increase in propagation delay. Beyond that, there is an increase in propagation delay although the curve appears "saturated." From corner to corner, we can see an increase in delay by approximately a factor of 4. Even for relatively small distances, the combination of Row and Column position can result in a doubling of the propagation delay.

The "wire" drawn on the schematic does not appear as a wire electrically, in this FPGA.

RH1020 P&R Analysis
Effect of Column Position on Prop Delay
May 17, 2000

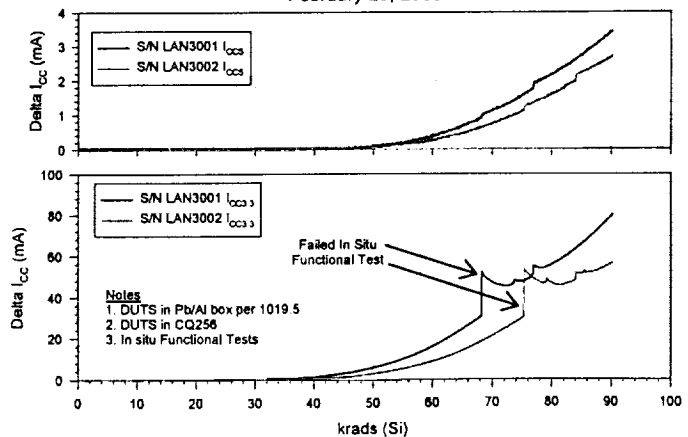


In Situ Functional Testing

For many of the older FPGA technologies, *in situ* monitoring of device current was in general a good indicator of the device's state. With some of the more modern technologies, as was the case with the A500K050 discussed above, we saw that functional failure and parametric shifts could occur without a large increase in supply current. The RAMTRON FRAM parallel RAMs also exhibited this property.

The chart below shows data for two production RT54SX16's, L/C P006. We see that at moderate current levels, failure was detected by our *in situ* functional monitor. The coverage for this test was high. Functional tests were run every krad(Si) of exposure.

RT54SX16 TID TEST
D/C 9937 - L/C P06/007
1 krad (Si) / Hour
NASA/GSFC
February 29, 2000



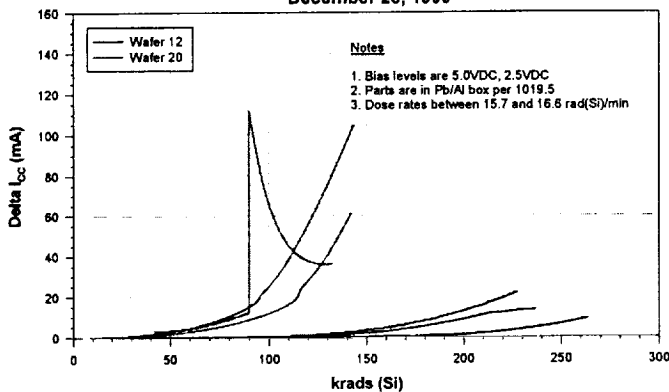
Clearly, one should never extrapolate the results of total dose radiation tests.

SX-A Technology

The SX technology consisted of "RT" parts produced at 0.6 μm at the MEC foundry and commercial grade parts fabricated at 0.35 μm technology at the Chartered Semiconductor foundry. The SX-A series devices are produced at 0.25 μm at MEC and at 0.22 μm at UMC. While the SX-series devices ran with a core voltage of 3.3 VDC, the SX-A-series devices run with a core voltage of 2.5 VDC. There are other electrical differences, such as in the I/O stage.

This note will review some of the total dose data from prototype MEC devices. An experiment was run on two wafers of A54SX32A (prototype) devices, produced at the MEC foundry. The two wafers were processed to see the effects on total dose performance. The bias voltages for this test consisted of 2.5 VDC for the array and 5.0 VDC for the I/O ring. Three parts from each of the two wafers were tested. Clearly, either of the two wafers would be considered radiation-tolerant. Wafer 20 demonstrated performance levels greater than 200 krad(Si). The results are summarized in the chart below.

A54SX32A (Prototype) TID TEST
D/C 9924
P04 Wafer 12 and 20
NASA/GSFC
December 28, 1999

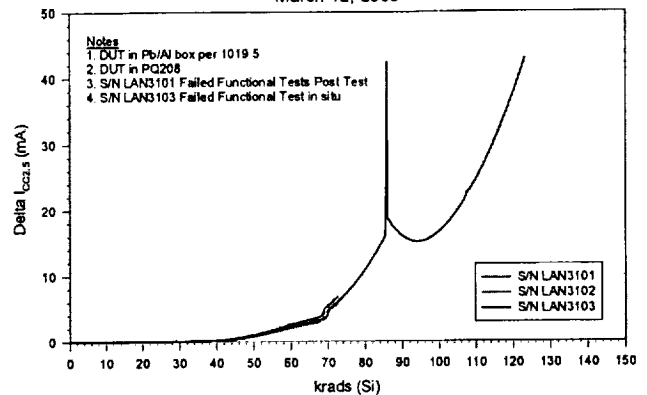


The two charts below summarize performance of 0.22 μm SX-A technology from the UMC fab. Again, with the use of *in situ* testing, it was shown that functional failure occurred with the small current jump seen in the strip chart. Note the low absolute level of the current when this failure was detected.

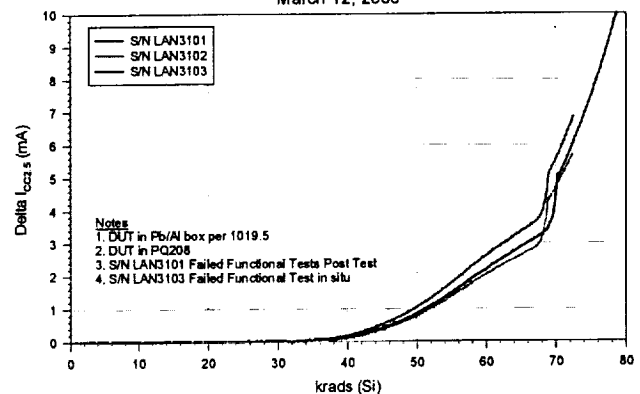
A42MX36 Heavy Ion Test

Previous heavy ion tests have shown that the A32200DX, with dual-port RAM, was highly

UKJ1822 TID TEST
A54SX32A Prototype (0.22 μm , UMC)
D/C 9951 - L/C D7584.8 #23
1 krad (Si) / Hour
NASA/GSFC
March 12, 2000



UKJ1822 TID TEST
A54SX32A Prototype (0.22 μm , UMC)
D/C 9951 - L/C D7584.8 #23
1 krad (Si) / Hour
NASA/GSFC
March 12, 2000

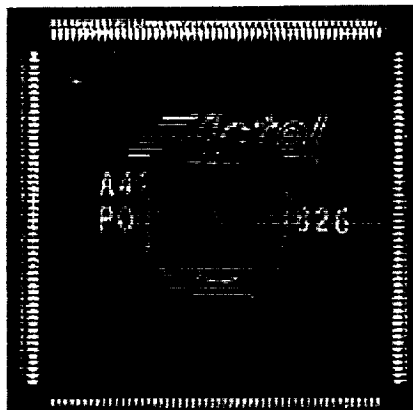


susceptible to single event latchup (SEL). No SEL was detected in the A32140DX, which did not include the SRAM. The A42MX36 is the direct descendant of the A32200DX. These devices were tested at Brookhaven National Lab in September, 1999. Bromine was used at normal incidence, for an LET = 38.1 MeV-cm²/mg. V_{CC} was set to a nominal 5.0 VDC. All runs resulted in the device latching, almost instantly. An attempt was made to find the latchup sensitive region by masking the part; this effort failed. Because of the low LET latchup, cross-section information and latchup threshold was not measured. A flux of approximately 1.2 x 10⁵ p/cm²/sec was used for all runs. Latchup currents, for some runs, exceeded two amps.

The devices were packed in a PQFP208. The D/C was 9826 and the lot code was 2ACT14014.1

More detailed information on this test is available at:

http://rk.gsfc.nasa.gov/richcontent/fpga_content/MX_Series/42MX36_BNL0999/42MX36_BNL0999.htm



National LVDS

LVDS DS90C031 Heavy Ion SEL Test
Brookhaven National Labs
September, 1999

Test Results Summary

Heavy ion tests were run on the National Semiconductor DS90C031 LVDS driver. These devices were modified to eliminate the latchup sensitivity they have shown in previous versions and heavy ion tests. The DUTs for this test were in flat packs and mounted on a controlled impedance (100 Ω) printed circuit board. Previous tests used SOIC and LCC packages. The dies are identified as DS90C031D by optical examination using a microscope.

No latchups were observed during these test runs. Three units were tested and all runs were at maximum voltage (5.5 VDC), worst-case for the single event latchup (SEL) test. Both data patterns (zeros and ones) were used. High fluences were used, typically 4×10^7 ions/cm² per run, to ensure a thorough test of this modified device. No functional failures or damage was detected.

Some Single Event Transient (SET) data was obtained. A graph of SET Cross-section vs. LET was not made since the parts were not tested at either nominal or low voltage. Hence, the data is supplied only for reference. The circuit configuration may also underestimate the SET rate; the four driver receiver pairs per device are wired in series. The output of the last receiver (DS90C032) is monitored in two ways. The first simply goes to a relatively

slow RS-422 driver, a DS26C31, which sends the signal down a long cable (50 to 100 feet twisted pair), into a DS26C32 RS-422 receiver, then into a counter implemented in an Altera 5192. The final contents of this counter are listed in "Upsets Slow." We expected, and observed, that the slow interface would act as a filter. The clock input of a 74AC109 was used as a fast transient pulse detector. This data is shown in the column labeled "Upsets All" and is a better indicator of the SET rate. It will underestimate a bit as the 4 series connected driver-receiver pairs may act as a filter.

Beam time limitations during this trip prevented a full SET characterization as well as testing at lower LETs to find the SET threshold - the primary objective of this test was to verify the SEL design fix. Our next test will perform an SET characterization. Additionally, transient waveforms will be captured to determine pulse amplitudes and widths.

For additional information, tables, and plots, please see:

http://rk.gsfc.nasa.gov/richcontent/Misc_Content/LV_DS/LVDS_September_1999.htm

Long Term Anneal

To investigate the effects of processing on total dose performance, the UCL064 lot of A14100A (0.8 μ m, MEC) was split several ways. Parts were selected from different wafers and exposed to 20 krad(Si) for this part of the test. The parts were then put on a long-term anneal; at the time of this writing, this has been 300 days. The two charts below summarize this information.

As can be seen, even at the modest level of 20 krad(Si), both sets of parts consumed relatively high levels of I_{CC} , with significant differences between the lot splits. With regular processing, over 125 mA was consumed while that figure dropped to about 20 mA for the modified process.

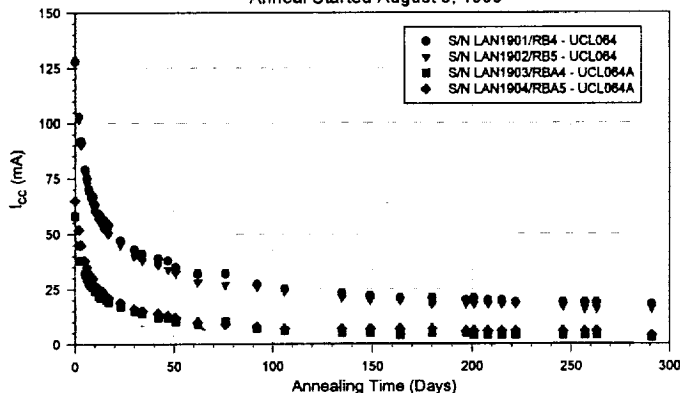
For the anneal, we see the drop in I_{CC} quickly tapering off, with the standard parts still consuming close to 20 mA and the modified parts consuming just a few mA.

The two charts are generated from the data same data set. The top chart presents the information in the usual linear-linear graph. The bottom chart presents the data in a log-log format where there appears to be a linear relationship between $\log_{10}(I_{CC})$ and

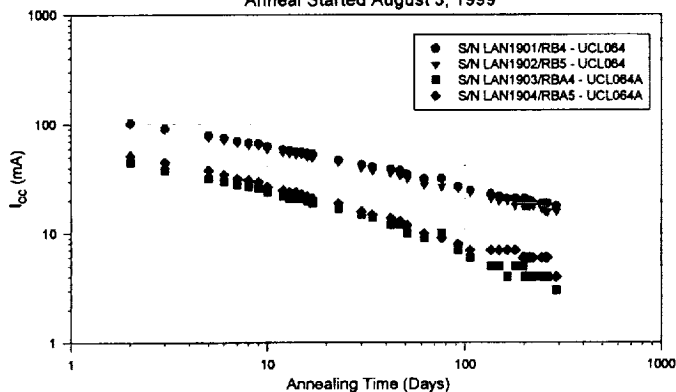
$\log_{10}(\text{Time})$. It is tempting to be able to extrapolate results from future tests, as these long term tests are time consuming, monopolize equipment, and are expensive. More data and analysis would be needed before extrapolation is possible.

Another set of long term annealing data is being taken on parts from the RT54SX series of devices.

A14100A/MEC TID TEST - Room Temp Anneal
D/C 9849 - UCL064 Lot Split
Post 20 krad(Si) Exposure @ 2.45 rad (Si) / Minute
NASA/GSFC
Anneal Started August 3, 1999



A14100A/MEC TID TEST - Room Temp Anneal
D/C 9849 - UCL064 Lot Split
Post 20 krad(Si) Exposure @ 2.45 rad (Si) / Minute
NASA/GSFC
Anneal Started August 3, 1999



KPP - A VHDL Pre-Processor

KPP is a pre-processor, similar to CPP, written for VHDL applications. It provides many standard functions such as `#def`, `#undef`, `#ifdef`, and `#include` that are often useful but not supported by VHDL. Other features are also provided such as for loops. This software will run on Win '95, Win '98, and Win NT and was written by Ingrid Brill.

For more information and the software, please see:

http://rk.gsfc.nasa.gov/richcontent/Software_Content/KPP.htm

Some information from the included help file shows some of the features of KPP.

define <variable> {number}: Causes the variable to be defined, or exist, in the program.

If number is included, the variable is defined as that number throughout the rest of the program.

#undef <variable>: Causes the variable to be undefined, or not exist, in the program.

#include <filename>: Replaces itself with the contents of the file filename (which are then also processed in the same fashion as the original code).

Nested `#includes` are allowed.

#ifdef <variable>: Performs the code below if the variable is defined.

#ifndef <variable>: Performs the code below if the variable is not defined.

#else: Must always have either an `#ifdef` or `#ifndef` preceding it. Performs the code below if the preceding `#ifdef` or `#ifndef` statement was false.

#endif: Needs to follow either an `#ifdef`, `#ifndef`, or an `#else`.

#for <variable> = x to y: Loops through the code below, letting variable equal all the numbers between x and y, with an increment of 1.

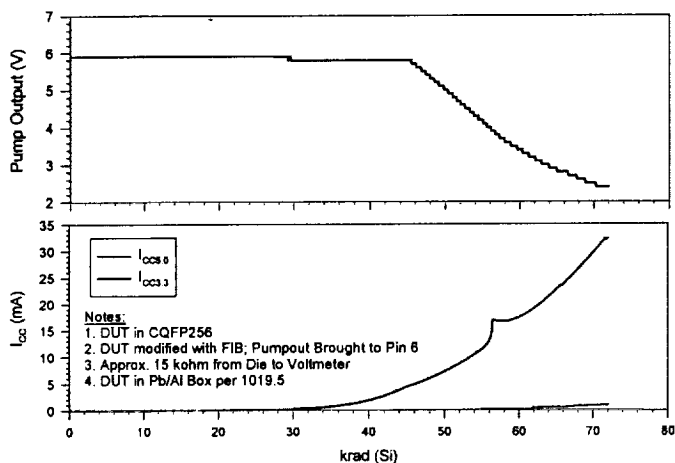
#endfor: Needs to follow a `#for`.

Charge Pump Measurements

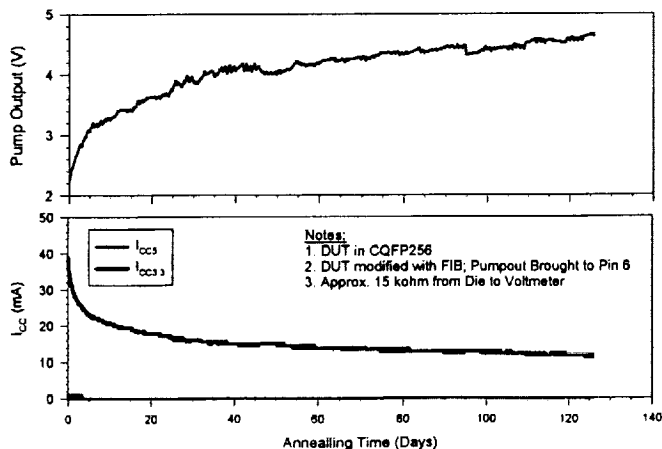
It has been known for a considerable period of time that radiation effects on the charge pump circuitry have major effects on certain classes of programmable devices. Largely, this was inferred. Using RT54SX technology, direct measurements are now available.

The RT54SX16 (0.6 μm ., MEC) device was used for this test. Using a focused ion beam (FIB) the microcircuit was modified, bringing the charge pump's output to an unused I/O pin, where it was routed to our measurement system. *In situ* measurements were performed and the results are shown in the two charts below. Experience has shown that the small increase of I_{CC} is associated with functional failure in this technology.

RT54SX16 Charge Pump Test
1 krad(Si)/Hour
S/N LAN2601
December 20, 1999
NASA/GSFC



RT54SX16 Charge Pump Test
Annealling After 72 krad(Si)
S/N LAN2601
May 21, 2000
NASA/GSFC

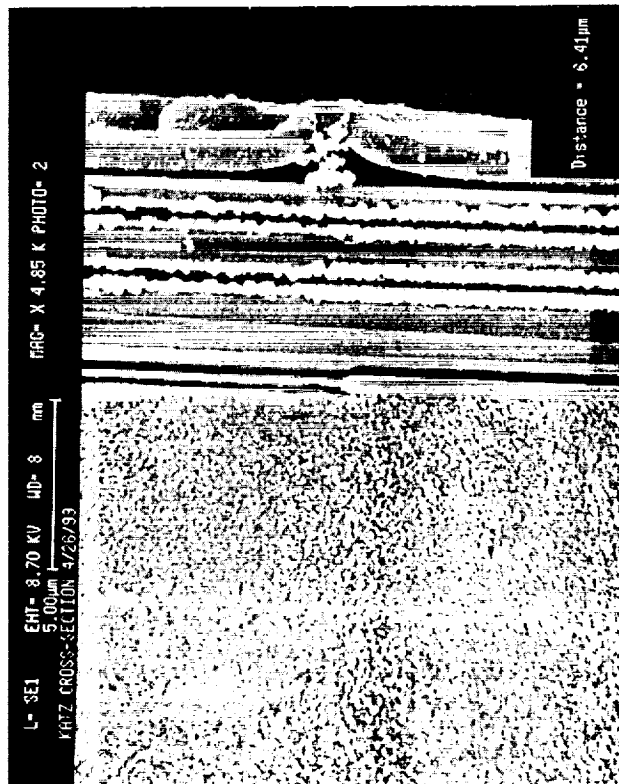


QL3025/EPI Experimental Devices

Heavy Ion Test

An experimental lot of QL3025's were fabricated, using an epitaxial layer of approximately 6.4 microns. Latchup tests were conducted at Brookhaven National Lab, using titanium at normal incidence, for an LET = 18.7 MeV-cm²/mg. Six devices were tested in total; three from each of two wafers. Nominal voltages for this part are V_{CCIO} = 5.0 VDC (input bias) and V_{CC} = 3.3VDC (majority of the part). Low voltage operation was also tested, attempting to find a latchup-free operating area. The results and current strip charts are shown on the www page referenced below. Because of the low LET latchup, cross-section information and latchup threshold was not measured

http://rk.gsfc.nasa.gov/richcontent/fpga_content/QuickLogic/QL3025EPI_BNL0499/QL3025EPI_BNL0499.htm



Total Dose Evaluation

Two of the experimental QL3025/epi devices were evaluated in the NASA/GSFC total dose test facility. Dose rates of 18.6 krad(Si)/Day and 1 krad(Si)/Day

were used. The results are summarized in the two charts below.

If we use the loss of control of the part as an estimate of the point of failure, we see a difference between the two dose rates of about 17%.

